I CLAIM:

1. A smart memory integrated-circuit device, comprising:

a memory array section;

a special-function section that is packaged with the memory array section in a single smart memory integrated-circuit package; and;

wherein said single smart memory integrated-circuit package incorporates all memory functions of a standard memory that are provided by the memory array section in addition to a special function that is provided by the special-function section in the single integrated-circuit package.

2. The smart memory of Claim 1 wherein the special-function section is connected to the memory array section through a common internal bus within the smart memory integrated-circuit package to thereby significantly reduce the need for the memory array section to communicate with another external, baseband integrated-circuit through an external common bus that has significantly greater propagation delay, parasitic capacitance, inductance, and resistance and that is required to be driven with higher current interface driving circuits.

3. The smart memory of Claim 1 wherein the single smart memory integrated-circuit package has substantially the same type, fit, and form of a package for only a conventional memory package that has only the memory array without the special function section.

4. The smart memory of Claim 1 wherein the special function section provides one or more memory-intensive functions.

5. The smart memory of Claim 1 wherein the smart memory integrated-circuit package is adapted to replace a standard memory product in a wireless appliance and is also adapted to incorporate the special function section into a standard memory package and thereby not requiring an additional special function IC; the need to have a more powerful baseband chip; or the need to significantly alter wireless appliance hardware, software, system architecture, and a printed-circuit design to which the single package is mounted in the wireless appliance.

6. The smart memory of Claim 1 wherein the memory array section and the special-function section are formed together monolithically as a single integrated-circuit chip.

7. The smart memory of Claim 6 wherein the memory array section and the special-function section are formed on a single integrated circuit with the same fabrication process.

8. The smart memory package of Claim 1 wherein the memory array section and the special-function section are provided as separate integrated-circuit chips that are contained in the same smart-memory package.

9. The smart memory of Claim 1 wherein the special-function section and the memory array section operates on an internal voltage supply level that is lower than an external voltage supply level for the smart memory integrated-circuit package.

10. The smart memory of Claim 1 wherein the special-function section is selected from a group consisting of: a high-fidelity audio system, a multi-media codec, a wireless short-distance communication system, , streaming video system, a wireless LAN, a Global Positioning System, and a video display.

11. The smart memory of Claim 1 wherein the memory array section is selected from a group consisting of: a SRAM, a pseudo-SRAM, a DRAM, an EEPROM, an EPROM, a FLASH, a RAM/FLASH combination, a RAM/FLASH/ROM combination, a ferroelectric RAM, and a magneto-RAM.

12. The smart memory of Claim 1 wherein the smart memory package type is selected from a group consisting of: a ball grid array BGA package, a quad flat pack QFP, a pin grid array package, and a multi-chip-module MCM package.

13. A smart memory integrated-circuit device, comprising:

a memory array section;

a special-function section that is packaged with the memory array section in a single smart memory integrated-circuit package;

wherein said single smart memory integrated-circuit package incorporates all memory functions of a standard memory that are provided by the memory array section in addition to a special function that is provided by the special-function section in the single integrated-circuit package;

wherein the special-function section is connected to the memory array section through a common internal bus within the smart memory integrated-circuit package; and

wherein the single smart memory integrated-circuit package has substantially the same type, fit, and form of a package for only a conventional memory package that has only the memory array section without the special function section.

(Amended)

14. A multi-media RAM (MMRAM) on a single integrated-circuit chip, comprising:

a memory array section formed on the single integrated-circuit die and contained in a multi-media RAM package;

a compressor/decompressor (CODEC) section integrally formed on the same single integrated-circuit die and contained in the same multi-media RAM package as the conventional memory array section, said CODEC section formed on the same single integrated-circuit die with the same fabrication process as the memory array section; and

wherein connections between the memory array section and the CODEC section are on the single integrated-circuit die.

15. The multi-media RAM of Claim 14 wherein the CODEC section is provided as hardwired logic circuits on the single integrated-circuit die.

16. The multi-media RAM of Claim 14 wherein data retrieval and data compression/decompression are performed within the single integrated-circuit chip without using high current input/output interface circuits.

17. The multi-media RAM of Claim 14 wherein the single integrated-circuit die is adapted for use in a wireless device that has a baseband DSP IC and wherein the single IC die is adapted to have minimal I/O interfacing with the baseband DSP IC in said wireless device such that the processing data rate of the baseband DSP IC is thereby reduced.

18. The multi-media RAM of Claim 14 wherein the CODEC is provided with a digital signal processor on the single integrated circuit die.

19. The multi-media RAM of Claim 18 wherein the CODEC is provided as a digital signal processor with a microcontroller on the single integrated-circuit chip.

20. The multi-media RAM of Claim 18 wherein the package for the single integrated-circuit chip is substantially the same as the package for a conventional memory array formed on the single integrated-circuit die.

21. The multi-media RAM of Claim 14 wherein the multi-media RAM package incorporates the special function section into a standard memory package that is adapted to replace a standard memory product in a wireless appliance and thereby does not require an additional special function IC; a more powerful baseband chip; or significant alterations to the wireless appliance hardware, software, system architecture, and printed-circuit design to which the single package is mounted in the wireless appliance.

22. The multi-media RAM of Claim 14 wherein the memory array section and the special-function section are formed together monolithically as a single integrated circuit chip.

23. A method of enhancing the capability of an integrated-circuit memory, comprising:

packaging a memory array section together with a special-function section in a single smart-memory integrated-circuit package; and

incorporating in the single smart-memory integrated-circuit package all of the memory functions of a standard memory that are provided by the memory array section in addition to incorporating a special function that is provided by the special function section;

whereby the single smart-memory integrated-circuit package is adapted to replace a standard memory product in a wireless appliance and to incorporate the special-function section in the smart-memory integrated-circuit package without requiring an

additional special function IC, without the need to have a more powerful baseband chip, or without the need to significantly alter wireless appliance hardware, software, system architecture, and a printed-circuit design to which the single package is mounted in the wireless appliance.

24. The method of Claim 23 including connecting the special-function section with the memory array section through a common internal bus within the smart-memory integrated-circuit package to significantly reduce the need for the memory array section to communicate with an external, baseband integrated-circuit over a common external bus that has significant propagation delay, parasitic capacitance, inductance, and resistance that further necessitate high current interface driving circuits.

25. The method of Claim 23 including packaging the memory array section and the special-function section in a single smart-memory integrated-circuit package that has a type, fit, and form of a conventional, standard memory package for the memory array section without the special-function section.

26. The method of Claim 23 including forming the memory array section and the special-function section together as a single integrated-circuit chip.

27. The method of Claim 26 including forming the memory array section and the special-function section on a single die using the same fabrication process.

28. The method of Claim 23 including forming the memory array section and the special-function section as separate integrated-circuit chips that are packaged together in the single smart-memory integrated-circuit package.

29. The method of Claim 23 including operating the special function section on an internal voltage supply level that is lower than an external voltage supply level for the smart-memory integrated-circuit package.

30. The method of Claim 23 wherein the special-function section is selected from a group consisting of: a high-fidelity audio system, a multi-media codec, a wireless short-distance communication system, , streaming video system, a wireless LAN, a Global Positioning System, and a video display.

31. The method of Claim 23 wherein the memory array section is selected from a group consisting of: a SRAM, a pseudo-SRAM, a DRAM, an EEPROM, an EPROM, a FLASH, a RAM/FLASH combination, a RAM/FLASH/ROM combination, a ferroelectric RAM, and a magneto-RAM.